METHOD AND APPARATUS FOR CORRECTING THE PHASE OF A CLOCK IN A DATA RECEIVER

Field of Invention

The invention relates to a method for correcting the phase of a clock in a data receiver and to an apparatus for carrying out the method particularly in an early-late phase detector.

Background of Invention

Data receivers often receive distorted signals, particularly in long distance transmission systems at high bit rates, for instance over standard signal fibre cables. Here, inter-symbol interference (ISI), chromatic dispersion (CD), polarisation mode dispersion (PMD), transmitter chirp, extinction ratio, fibre non-linearity may occur and result in the so-called reduced eye opening. The incoming data at the receiver can be considered as a varying analogue signal from which a timing or clock information can be recovered which is necessary to sample the incoming signal at appropriate intervals to recover the data. This function is commonly accomplished with the aid of a phase locked loop (PLL) which includes a phase detector (PD), a loop filter (LF) and a voltage controlled oscillator (VCO). A well-known phase detector is the early-late phase detector described by Alexander. This detector generates output signals which indicate the direction of the phase deviation relative to a correct timing. These output signals are termed "up" and "down" control signals. The incoming signal which carries the data flow has logical signal values which generally are termed 1 or 0. Between adjacent logical signal values a signal transition may happen. The Alexander phase detector samples two adjacent logical signal values and the signal transition therebetween, these sampled signals being termed "a sample group" in this application. If the sample values which may be 1 or 0 are different among adjacent logical signal values, sampling the signal transition between these adjacent logical signal values may result in a 1 or 0. If the first logical signal value of a group and the signal transition value are equal and

differ from the value of the second logical signal value, the clock is too early, and if the signal transition value and the second logical signal value are equal, the clock is too late. In the first case the clock is to slow down and in the second case to speed up. The output signal of the phase detector is converted by the loop filter and fed to the voltage controlled oscillator for controlling the output clock frequency thereof. The clock is fed back to the phase detector and determine the sampling intervals by the position of the rising (or falling)edges of the clock frequency signal. Statistically up and down control signals will happen equally so that the sampling phase controlled by the clock frequency will be correctly adapted to the incoming signal carrying the data flow.

If there are large signal distortions in the incoming data flow, it becomes difficult to correct the phase of the clock in the data receiver, since the performance of the early-late phase detector is degraded and the phase locked loop fails to lock. This is true especially for partial response channels, where differential group delay occurs approximately at the bit transition, the phase detector does not succeed in finding a stable sampling clock phase.

Summary of the Invention

An object of the invention is to correct the phase of a clock in a data receiver also if the incoming signals of the data flow are strongly distorted.

The invention is based on the principle that the logical high and low signal values that represent the bits in the data flow follow randomly, i.e. an incoming signal with sufficient duration statistically will have sections where a pair of high signal values is followed by a pair of low signal values or a pair of low signal values is followed by a pair of high signal values. These signal sections commonly are distorted to a lesser degree, and the chance to find the signal transition correctly is enhanced. The invention makes use of this circumstance and weights such signal transitions stronger than for all findings of other signal transitions.

With the invention, also an improved phase detector is created. An

early-late phase detector of prior art is modified in that the output stage is enabled to produce two different output signals, one for standard operation and another with a scaling or amplification factor, for the signal transitions between pairs of signal values of different levels.

The invention can be implemented at low additional costs to that of a standard early-late phase detector. Circuitry may be realised in digital technology. Only one gate level is needed for high speed applications. The gate circuitry can be implemented with low costs and on small size. Testing of the circuitry is uncritical, because no feed back loops are needed in the gate circuitry. The behaviour is deterministic and this can be validated.

With the invention, locking of the receiver on the incoming data flow is improved also if the incoming signals are distorted. The output signal of the early-late phase detector is weighted and by setting the weight factor on an appropriate value (for instance 4) a trade-off between fast acquisition, jitter of the receive phase locked loop and stable lock can be found.

Brief description of the drawings

Fig 1. is an eye opening diagram for distorted signals.

Fig. 2 is a block diagram of a receive phase locked loop.

Fig. 3 is a signal and clock scheme for showing phase detection timing and

Fig. 4 is a block diagram of an early-late phase detector improved according to the invention.

Description of the preferred embodiments

Fig. 2 shows the phase locked loop in an data receiver including a phase detector PD , a loop filter LF and an analogue voltage controlled oscillator VCO. The incoming data flow is indicated at "data in". The output of the voltage controlled oscillator VCO is indicated with "clock". The circuit functions to sample the incoming data with the clock frequency and to recover timing information for the voltage controlled oscillator VCO to generate the correct clock frequency with the correct phase for sampling the incoming signal.

Fig. 3 shows controlled by the clock CLK sampling times AA, A, T, B and BB for the incoming data flow. Times AA, A, B and BB are in intervals of one bit, whereas time T is at signal transition between two adjacent bits at times A and B in the data flow. The signal samples at A, T and B form an "inner sample group" as used in a conventional early-late phase detector and the signal samples AA, A, T, B, BB form an "enlarged sample group" .Samples AA and A form a first signal sample pair and samples B and BB form a second signal sample pair.

Fig. 4 shows the circuitry for correcting the phase of the clock in the data receiver. The incoming data are connected to a first shift register SR1 and a second shift register SR2. Shift register SR1 has four flip flops in a row which form stages or cells which receive the sampling probes indicated in Fig. 3 and shift them from stage to stage in the timing of the clock. Shift register SR2 has three flip flops in a row which form stages or cells where the first cell in the row is addressed by the falling edge of the clock pulse so as to sample an expected signal transition and store it intermediately and shift it to the output of the shift register SR2 in a time period when sample probe A appears at the output of the third cell of shift register SR1.

The phase detector also includes a first gate circuit GC1 and a second gate circuit GC2. Gate circuit GC1 is configured in two rows where each row comprises an EXOR gate as input stage, an AND gate having one inverted input as the second stage, a flip flop as the third stage and a weighting output stage which delivers a control output to be delivered to the loop filter LF and hence to the voltage controlled oscillator VCO for controlling same. The output signal of the upper row is termed "UP" and of the lower row "DOWN". UP means shifting the edges of the clock CLK to the left in Fig. 3 and DOWN means shifting to the right hand side. The output stages of the gate circuit GC1, each comprises a second input (SI) from gate Circuit GC2 which can switch the output stage into a condition of multiplying the output signal UP or DOWN by a scaling or amplification factor x which

has a value between 1 and 4. Further circuitry (not shown) may evaluate the quality of the incoming data signal and deliver a setting signal to set the value of factor x at an appropriate level.

Gate circuit GC2 has a pair of EXNOR gates at the input, an AND gate connected to the outputs of the EXNOR gates and a flip flop as output stage provided for timing purposes and being connected to the output stages of the first gate circuit GC1.

The conventional early-late phase detector of Alexander is indicated at APD in Fig. 4, wherein the symbols BB and B are to be exchanged for B and A. The operation of the detector APD can best be understood from table 1 wherein the signal samples are taken at times A, T and B. The signal value can be "high" indicated by 1, or "low" indicated by 0.

The signal transition at time T may have a value which is nearer to low, then the sample value is 0, or nearer to high, then the sample value is 1. There are patterns of the signal samples which produce an output for controlling the voltage controlled oscillator VCO, and patterns from which no information for controlling the VVO can be derived. (Output UP =0, DOWN=0).

The latter pattern includes the signal samples 010 and 101 which mean highly distorted signals. Such signals are shown schematically in Fig 1 with the thin line thickness. Distortions may also lead to patterns of signal samples which produce outputs with the wrong direction of phase correction. In such situations, the phase detector does not succeed in finding a stable sampling clock phase.

Signals carrying a data flow may show data bit patterns with a pair of 11 and a pair of 00 and a transition between such pairs. Also data bit patterns 00 followed by 11 are possible. In signal sections with such bit pairs, the transitions between the pairs may be termed "half rate transitions". These half rate transitions produce Eye openings shown at the left hand side and right hand side of Fig. 1. Finding these half rate transitions and using

them for clock control will result in a good phase correction. The novel features of the early-late phase detector of the invention lead to these excellent characteristics.

Table 2 shows signal samples at sampling times AA, A, T, B, BB, the logical equations belonging thereto and the output signal from the improved early-late phase detector. As shown, the improved detector is able to find signal patterns with pairs of signal values having the same signal levels "high" or "low". The signal transition between adjacent pairs may be high (1) or low (0). In any case, such patterns of signal samples are valuable to control the VCO and therefore are stronger weighted than any other patterns. The circuitry for doing so has already been explained with Fig. 4.

Logical Equations	Signal Samples	Output
A=T AND B/=T	001,110	down = 1 up = 0
A/=B AND B=T	011,100	up = 1 down = 0
Others	000,010,101,111	up = 0 down = 0

Table 1

Logical Equations		Sample Groups	Output
A=T AND B/=T	A=AA AND B=BB	00011,11100	down = x
A/=B AND B=T		00111,11000	up = x
A=T AND B/=T	A/=AA OR B/=BB	00010,10011,10010, 11101,01100,01101	down = 1
A/=B AND B=T		00110,10111,10110 11001,01000,01001	up = 1
Others		00000,00001,10000,10001 00100,00101,10100,10101 01010,01011,11010,11011 01110,01111,11110,11111	up = 0 down = 0

Table 2